REMARKS/ARGUMENTS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 219-223, 228, 232, 236, 238-242, 250-257, 259, 260 and 262-267 are pending; Claims 219, 220, 223, 232, 236, 250-252, 256, 257, 260, 262-264, 266 and 267 have been currently amended; Claims 1-218, 224-227, 229-231, 233-235, 237, 243-249, 258 and 261 are canceled.

Response to Claim Rejections under 35 U.S.C. 112

Reconsiderations of Claims 220, 263 and 267 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention are requested based on the following remarks.

The element of "first patterned circuit layer" is recited in line 8 of independent Claim 219. Thus, there is an antecedent basis for "said first patterned circuit layer" in dependent Claims 220, 263 and 267.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 219-223, 228-236, 238-242, 250-257, 259, 260 and 262-267

As currently amended, independent claim 219 is recited below:

219. A chip package comprising:

a substrate comprising semiconductor material;

only one die;

an adhesive material joining said substrate and said only one die;

a first insulating layer comprising a first portion over said only one die and a second portion over said substrate but not over said only one die, wherein said first insulating layer comprises polyimide; and

a first patterned circuit layer over said first insulating layer.

Section I

Reconsiderations of Claims 219-223, 228-236, 250, 251, 257, 259, 260, 263, 264, 266 and 267 rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama (US2001/0042901) in combination with Ahn et al. (US2003/0020180), of Claim 262 rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama in combination with Alcoe et al. (US2002/0135063), and of Claim 265 rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama in combination with MacIntyre (US6,555,469) are requested based on the following remarks.

Applicants respectfully assert that the chip package claimed in Claim 219 patentably distinguishes over the citations by Maruyama (US2001/0042901) in combination with Ahn et al. (US2003/0020180).

Maruyama teaches a semiconductor wafer 11 provided with multiple circuit regions 12, an insulating layer 20, such as SiO2, over the semiconductor wafer 11, and a patterned circuit layer 15 over the insulating layer 20. ~ *See FIGS. 17A-17D and paragraphs*

[0168]-[170] ~

The Examiner considers that the reference number of 12 can be deemed as only one die. *~ See lines 3 and 4 in point 7, in the last Office Action mailed Mar. 13, 2007 ~*

Applicants respectfully traverse the Examiner's opinion because the reference number of 12 can not be deemed as only one die. "Die" is typically well-known as a body separated from "Wafer". The circuit regions 12 are in the semiconductor wafer 11 but not separated from the wafer 11. The circuit regions 12 are typically formed over a semiconductor substrate by a sputtering process, for example, during forming the semiconductor wafer 11. A die is provided by separating the semiconductor wafer 11 after being formed with the circuit regions 12.

Furthermore, the semiconductor wafer 11 has multiple circuit regions 12, which is believed not to be deemed as only one preformed die, as claimed in Claim 219.

The Examiner concurs that the definition of "Die" is different from that of "Wafer", but considers that "structurally as claimed there is no difference between defined circuit regions/dice in a wafer and a die that is on a cavity within a wafer or substrate". *~ See lines 2-7, in point 45, in the last Office Action mailed Mar. 13, 2007 ~*

Applicants respectfully traverse the Examiner's opinion because structurally as claimed there is some difference between defined circuit regions/dice in a wafer and a die that is on a cavity within a wafer or substrate. The process for forming the circuit regions 12 on the semiconductor wafer 11 is not using an adhesive material to join the circuit regions 12 and the semiconductor wafer 11. In a structural view, an adhesive material joining the circuit regions 12 and the semiconductor wafer 11 is believed not to be found in Maruyama's device.

The subject matter of "an adhesive material joining a substrate and only one die", as claimed in Claim 210, is not taught by Maruyama even in view of Ahn et al.

As a result, withdrawal of rejection under 35 U.S.C. 103(a) to Claim 219 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 219 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 220-223, 228-236, 238-242, 250-257, 259, 260 and 262-267 patently define over the prior art as well.

Section II

Reconsiderations of Claims 219-223, 228-236, 238, 239, 250, 251, 257, 257, 259, 260 and 263-267 rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi (US6,867,499) and Ahn (US2003/0020180), of Claim 240 rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi and Ahn further in combination with Tahara et al. (US2002/0017730), of Claim 241 rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi and Ahn further in combination with Shuy et al. (US2003/0118738), of Claim 242 rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi and Ahn further in combination with Jun et al. (US2002/0084510), of Claims 252-256 rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi and Ahn further in combination with Korman (US5,959,357), and of Claim 262 rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi and Ahn further in combination with Alcoe et al. (US2002/0135063) are requested based on the following remarks.

Applicants respectfully assert that the chip package claimed in Claim 219 patentably distinguishes over the citations by Tabrizi (US6,867,499) in combination with

Ahn et al. (US2003/0020180).

Tabrizi teaches a chip package comprising a substrate 510 comprising semiconductor material; only one die 520; an adhesive material 530 joining said substrate 510 and said only one die 520; a first insulating layer 550 comprising a first portion over said only one die 520 and a second portion over said substrate 510 but not over said only one die 520; and a first patterned circuit layer 560 over said first insulating layer 550. ~ *See FIG. 5 and col. 4, lines 33-44* ~

Tabrizi teaches the first insulating layer 550 is bisbenzocyclobutene (BCB). ~ *See col. 3, lines 23 and 39-50* ~ However, Tabrizi fails to teach the first insulating layer 550 may comprises polyimide.

The Examiner considers that "Tabrizi discloses the same invention as claimed except that its insulation is disclosed as BCB instead of polyimide. Ahn (Par. 0036) shows that both BCB and polyimide produce equivalent structures known in the art. Therefore, because these two insulators are art recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to select polyimide for BCB insulator." ~ *See point 22, in the last Office Action mailed Mar. 13, 2007* ~

Applicants respectfully traverse the Examiner's opinion because one skilled in the art at the time of the invention would not readily recognize substituting polyimide in Ahn's device for said first insulating layer 550 in Tabrizi's device.

Even Ahn teaches "the intermetal dielectric layer 55 may be also formed of a conventional insulating oxide, such as silicon oxide (SiO_2), or other low-dielectric constant materials such as, for example, polyimide, spin-on-polymers (SOP), parylene,

flare, polyarylethers, polytetrafluoroethylene, benzocyclobutene (BCB), SILK, fluorinated silicon oxide (FSG), NANOGLASS or hydrogen silsesquioxane, which have dielectric constants of less than about 4. ~ *See lines 3-11, in para. [0036]* ~ However, Ahn fails to teach what kind of insulating layer can be formed over a structure constructed of a die joined with a preformed substrate using an adhesive material. Ahn has no motivation to form an insulating layer over a structure constructed of a die joined with a substrate using an adhesive material. As a result, it is believed that the dielectric layer 55 in Ahn's device is non-analogous to the insulating layer 550 in Tabrizi's device.

As a result, withdrawal of rejection under 35 U.S.C. 103(a) to Claim 219 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 219 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 220-223, 228-236, 238-242, 250-257, 259, 260 and 262-267 patently define over the prior art as well.

Conclusion

Some or all of the pending claims are believed to be in condition for Allowance, and that is so requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: 06.08.2007

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)